

Series Linear Regulator Controller

DESCRIPTION

SiP21301 is a single channel series regulator controller to drive N-Channel MOSFET. It is the perfect choice for the low voltage, high current application.

This controller provides the complete features, such as non-rush current on soft start-up, short circuit protection and thermal shutdown.

In addition, it has under-voltage lock-out for safe operation. SiP21301 is designed to maintain regulation while delivering up to 7 A peak current, making it ideal for systems that have a high surge current upon turn-on.

SiP21301 provides an adjustable output as well as fixed output voltage options 1.2 V and 1.5 V.

SiP21301 is available in a lead (Pb)-free MSOP8 package for operating over temperature range (- 10 °C to 100 °C).

FEATURES

- Programmable Non Rush Current on Start up (NRCS)
- Short Circuit Protection (SCP)
- Thermal Shutdown
- UVLO and Latch Function
- Fixed 1.2 V and 1.5 V Output Voltage Options
- N-Channel MOSFET driver
- MSOP8 Package

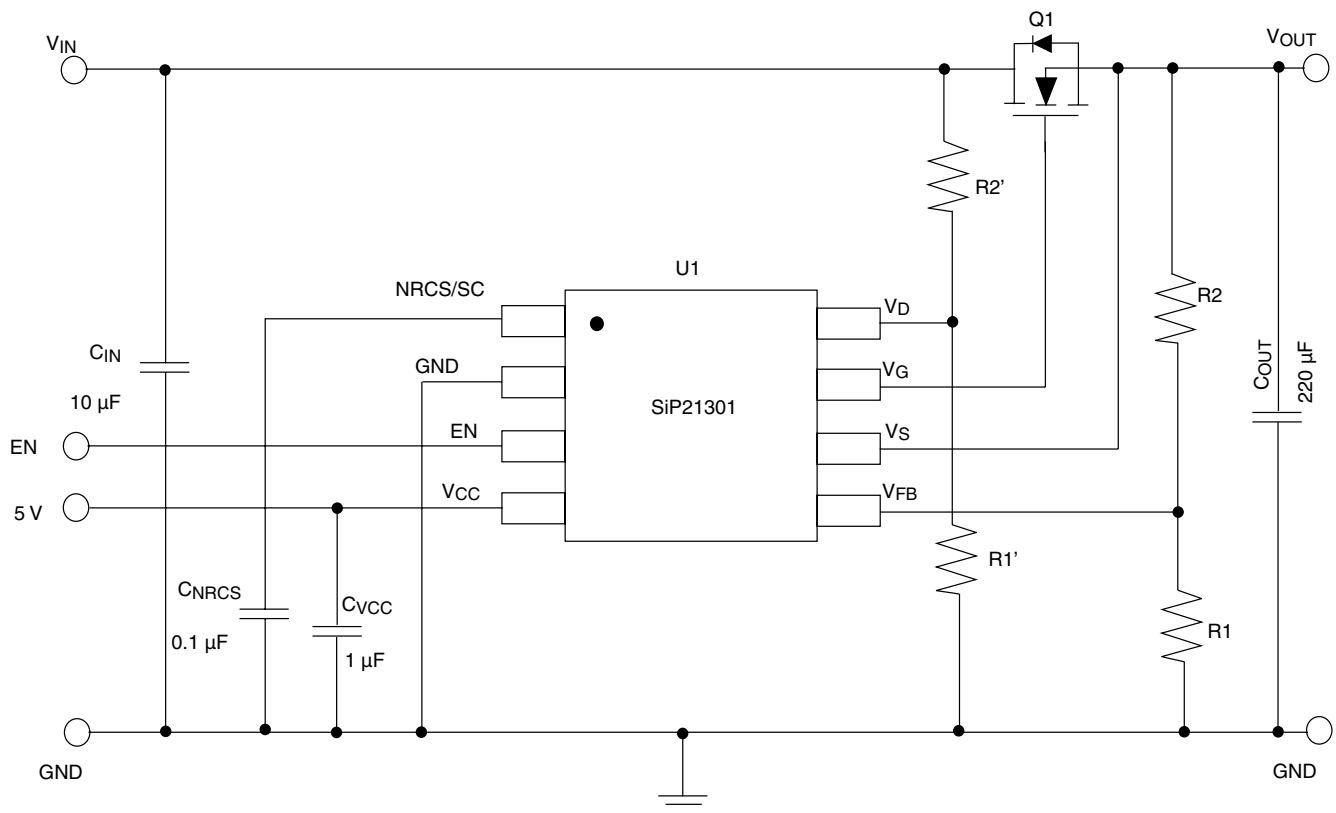


RoHS
COMPLIANT

APPLICATIONS

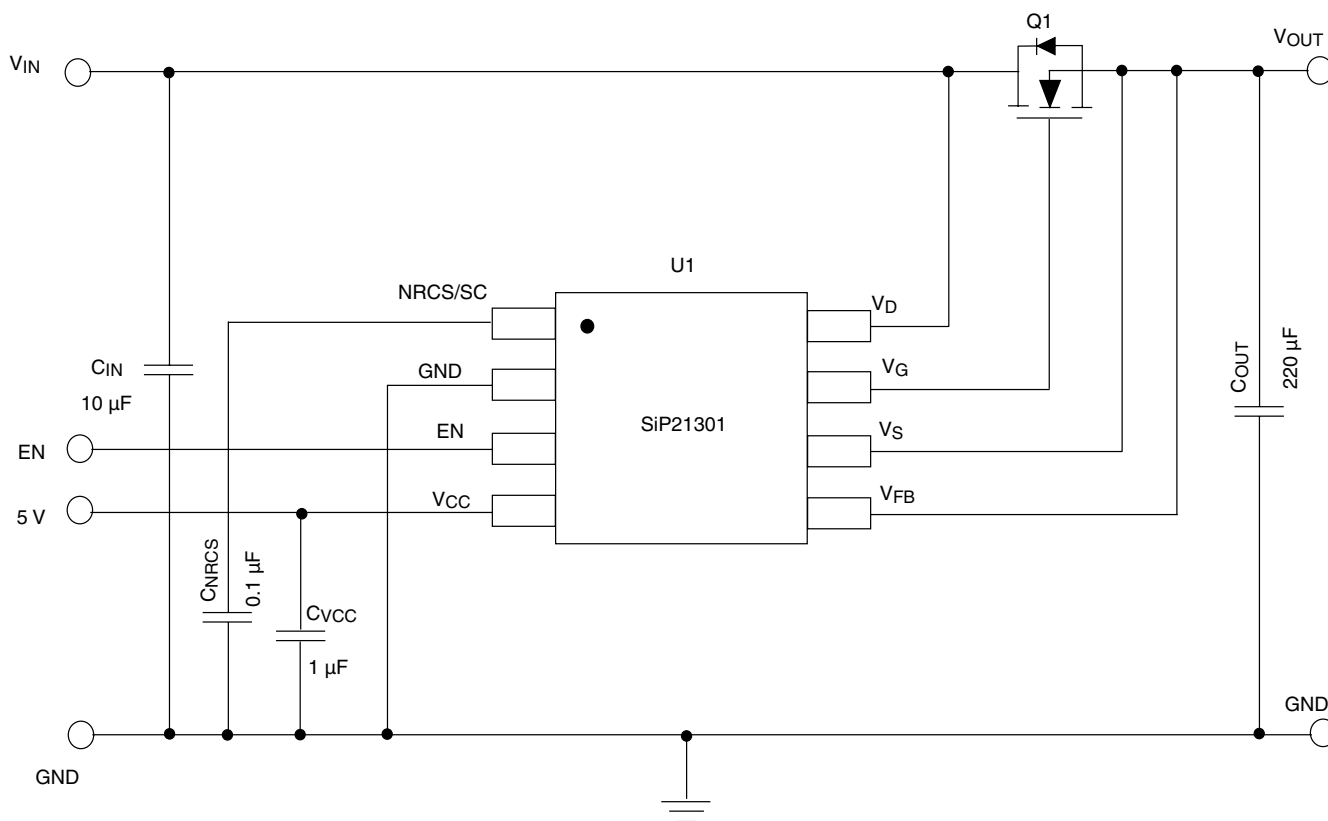
- Game Console
- Set Top Box

TYPICAL APPLICATION CIRCUIT



SiP21301 Adjustable Version

Figure 1.



SiP21301 - Fixed Version

Figure 2.

ABSOLUTE MAXIMUM RATINGS		
Parameter	Limit	Unit
Supply Input Voltage (V_{CC})	- 0.3 to 6	V
Drain Voltage (V_D)	- 0.3 to 6	
Enable Input Voltage (V_{EN})	- 0.3 to 6	
Power Dissipation ^a (P_d)	666	mW
Storage Temperature (T_{stg})	- 65 to 150	°C
Maximum Junction Temperature	150	
Package Thermal Resistance ^b (θ_{JA})	150	°C/W

Notes:

- a. Device mounted with all leads soldered or welded to PC board.
- b. Derate 6.6 mW/°C above $T_A = 25$ °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.



RECOMMENDED OPERATING RANGE		
Parameter	Limit	Unit
Supply Voltage (V_{CC})	4.5 to 5.5	V
Drain Voltage (V_D)	0.65 to 5.5	
Enable Input Voltage (V_{EN})	- 0.3 to 5.5	
Capacitor On NRCS/SCP Terminal (C_{NRCS})	0.001 to 1	μ f
Maximum Output Voltage Range (V_O)	0.65 to 2.5	V
Operating Temperature Range (T_{OPR})	- 10 to 100	$^{\circ}$ C

ELECTRICAL SPECIFICATIONS							
Parameter	Symbol	Test Conditions $V_{CC} = 5\text{ V}$, $V_D = V_{IN} = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$, $R1 = R1' = \infty\ \Omega$, $R2 = R2' = 0\ \Omega$ $T_A = 25\ ^{\circ}\text{C}$. Unless Otherwise Specified	Temp	Min ^a	Typ ^b	Max ^a	Unit
Supply Section							
Supply Current	I_{CC}		Room		1.0	1.7	mA
Shutdown Supply Current	I_{SD}	$V_{EN} = 0\text{ V}$	Room		0.1	10	μ A
Line Regulation	$\Delta V_O / \Delta V_{CC}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_O = 50\text{ mA}$	Room		0.1	0.5	%/V
Load Regulation	$\Delta V_O / \Delta I_O$	$I_O = 0\text{ A to } 3\text{ A}$	Room		0.5	10	mV
Adjustable Version Only							
Feedback Voltage 1	V_{FB1}	$I_O = 50\text{ mA}$	Room	0.643	0.650	0.657	V
Feedback Voltage 2	V_{FB2}	$I_O = 50\text{ mA}$, $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $T_A = -10\ ^{\circ}\text{C to } 100\ ^{\circ}\text{C}$	Full	0.634	0.650	0.666	
Output Voltage	V_O	$R1 = R1' = 3.9\text{ k}\Omega$ $R2 = R2' = 3.3\text{ k}\Omega$	Room		1.2		
V_{FB} Input Bias Current	I_{FB}		Room		80		nA
Fixed Version Only							
Feedback Voltage 1	V_{FB1}	$I_O = 50\text{ mA}$	Room	- 1.0	0	1.0	%
Feedback Voltage 2	V_{FB2}	$I_O = 50\text{ mA}$, $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $T_A = -10\ ^{\circ}\text{C to } 100\ ^{\circ}\text{C}$	Full	- 2.5	0	2.5	
Enable Section							
High Level Enable Input Voltage	V_{ENH}		Room	2			V
Low Level Enable Input Voltage	V_{ENL}		Room			0.8	
Enable Input Current	I_{EN}	$V_{EN} = 3\text{ V}$	Room		7	10	μ A
Source Section							
V_S Input Bias Current			Room		1.2	2.4	mA
V_S Stand-by Current			Room	150			
Output Drive Section (Adjustable Version Only)							
Driver Source Current	I_{GSO}	$V_{FB} = 0.6\text{ V}$, $V_G = 2.5\text{ V}$	Room	2	3	4	mA
Drive Sink Current	I_{GSI}	$V_{FB} = 0.7\text{ V}$, $V_G = 2.5\text{ V}$	Room	2	3	4	
Output Drive Section (Fixed version Only)							
Driver Source current	I_{GSO}	$V_{FB} = V_O - 0.1\text{ V}$, $V_G = 2.5\text{ V}$	Room	2	3	4	mA
Driver Sink Current	I_{GSI}	$V_{FB} = V_O + 0.1\text{ V}$, $V_G = 2.5\text{ V}$	Room	2	3	4	
UVLO Section							
V_{CC} UVLO	V_{CCUV}	V_{CC} : Sweep up	Room	4.20	4.35	4.50	V
V_{CC} UVLO Hysteresis	V_{CCHYS}	V_{CC} : Sweep down	Room	100	160	220	mV
V_D UVLO	V_{DUV}	V_D : Sweep up	Room	$0.6 \times V_O$	$0.7 \times V_O$	$0.8 \times V_O$	V

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Test Conditions	Temp	Min ^a	Typ ^b	Max ^a	Unit
		Unless Otherwise Specified					
Drain Voltage Sensing Section (Adjustable Version Only)							
V_D Input Bias Current	I_D	$V_{CC} = 5\text{ V}, V_D = V_{IN} = 3.3\text{ V}, V_{EN} = 3\text{ V},$ $R1 = R1' = \infty\ \Omega, R2 = R2' = 0\ \Omega$ $T_A = 25\text{ }^\circ\text{C}.$	Room		0		nA
Drain Voltage Sensing Section (Fixed Version Only)							
V_D Input Bias Current	I_D	$V_D = 3.3\text{ V}$	Room		100	200	μA
NRCS/SCP Section							
NRCS Charge Current	NRCS	$V_{NRCS/SCP} = 0.5\text{ V}$	Room	14	20	26	μA
SCP Charge Current	I_{SCP}	$V_{NRCS/SCP} = 0.5\text{ V}$	Room	14	20	26	
SCP Discharge Current	I_{SCPD}	$V_{NRCS/SCP} = 0.5\text{ V}$	Room	0.3			mA
SCP Threshold Voltage	V_{SCP}		Room	1.2	1.3	1.4	V
Short Detect Voltage	V_{OSCP}		Room	$V_O \times 0.3$	$V_O \times 0.35$	$V_O \times 0.4$	
NRCS Stand-by Voltage	V_{NS}		Room			50	mV

Notes:

- a. The algebraic convention whereby the most negative value is a minimum and most positive is a maximum.
 b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

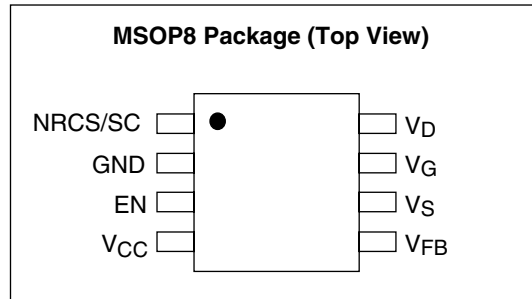
PIN CONFIGURATION

Figure 3.

PIN DESCRIPTION

Pin Number	Name	Function
1	NRCS/SCP	Non-rush current on Start-up/Short circuit protection
2	GND	Ground pin
3	EN	By applying less than 0.8 V to this pin, the device will be turned off Connect this pin to V_{CC} if unused
4	V_{CC}	Input supply pin
5	V_{FB}	Feedback input - Adjustable version: Connect feedback resistors to program the output voltage for the regulator - Fixed version: Connect this pin to V_S pin
6	V_S	Output of regulator. Connect to source of N-channel MOSFET
7	V_G	Connect to gate of N-Channel MOSFET
8	V_D	Connect to drain of N-Channel MOSFET

ORDERING INFORMATION			
Part Number	Marking	Temperature Range	Package
SiP21301LH-AD-E3	01AD	- 10 °C to 100 °C	MSOP8
SiP21301LH-12-E3	0112		
SiP21301LH-15-E3	0115		

FUNCTIONAL BLOCK DIAGRAM

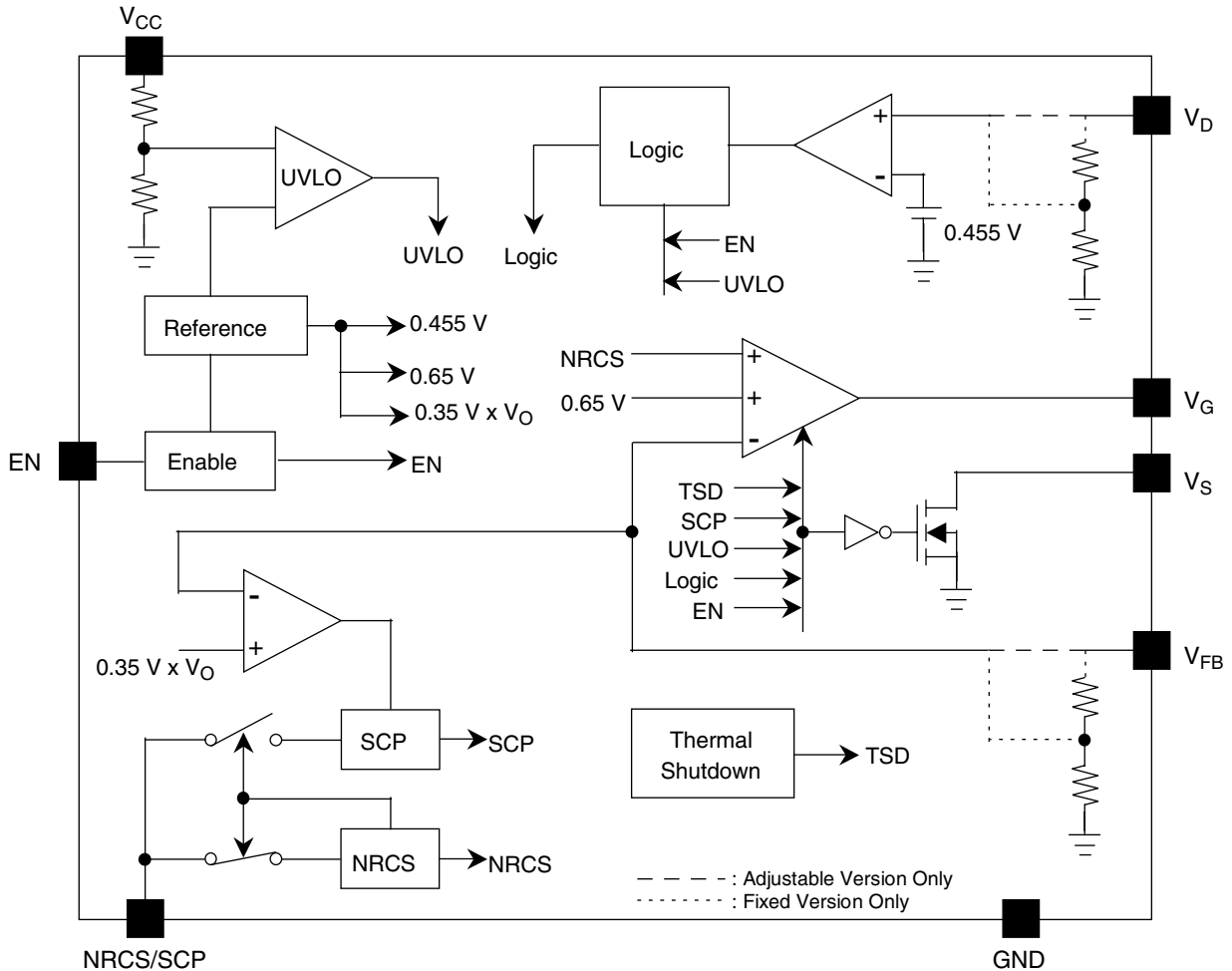


Figure 4.

DETAILED OPERATION DESCRIPTION

SiP21301 is the LDO controller for the low voltage, high current application. It consists of enable, device UVLO, LDO UVLO, thermal shutdown, NRCS (None Rush Current Start-up), SCP (LDO Output Short Circuit Protection), reference voltage and error amplifier.

ENABLE

The ENABLE block is to generate the enable and disable signal to turn the LDO control block on and off. If the voltage on EN pin is applied greater than 2.0 V, the control block are enable. If the voltage on EN pin applied less than 0.8 V, the control block are disabled. EN pin is an active high pin. When EN pin activates high, an internal 20 μ A current source will charge up the external NRCS/SCP capacitor with out any delay.

Reference Voltage

The reference voltage is enabled, when the enable active high signal is applied to the EN pin. The reference voltage block is composed of a self-biased shunt reference circuit and generates following several references to for the control block:

1. 1.0 V for the NRCS circuit
2. 0.455 V for LDO UVLO circuit
3. 1.3 V for short circuit protection circuit
4. 0.65 V for output regulation
5. $0.35 \times V_O$ for short circuit detection

Thermal Shutdown

SiP21301 has a thermal shutdown circuit to protection itself. When the junction temperature is around 175 $^{\circ}$ C, the thermal shutdown function is activated, the output jumps into shutdown mode.

Controller UVLO

The function of controller UVLO is the under-voltage lockout function for SiP21301 itself. This function block consists of an input detection circuit and UVLO circuit. The input detection circuit senses the voltage on V_{CC} pin to check for the safe operation for the rest of the control block. If the V_{CC} voltage is lower than 3.5 V, this V_{CC} detection circuit will make the output turn off to prevent improper operation of SiP21301. To drive an external N-Channel MOSFET without any charge pump circuit built-in as well as externally, it requires an enough voltage difference between V_{CC} and V_O to drive the external power MOSFET properly. The controller UVLO is built-in to ensure proper voltage difference between the gate and source of the external power MOSFET. The V_{CC} need to reach 4.35 V to unlock UVLO. It has 160 mV hysteresis.

LDO UVLO

The LDO UVLO checks the drain voltage of the external N-Channel MOSFET independently and guarantees the V_D voltage from abnormal condition. For fixed output version, the V_D pin is typically connected to the input of LDO. If the V_D voltage is greater than $0.7 \times V_O$, the LDO UVLO will be unlocked. For adjustable version, an external voltage divider is required to set the UVLO voltage in the input side of LDO.

The typical input UVLO threshold voltage is set to $0.7 \times V_O$. If the V_D voltage is greater than 0.455 V, the LDO UVLO will be unlocked.

NRCS

The NRCS circuit begins initiated when the EN pin active high and the voltage on NRCS/SCP pin begins to ramp up because the external NRCS/SCP capacitor is being charged up by an internal 20 μ A constant current source. When controller UVLO and LDO UVLO are released with 75 μ s delay, NRCS circuit completed initialization. The voltage on NRCS/SCP keeps ramping up to 1 V. Once it reaches 1 V, the voltage on NRCS/SCP starts to discharge to ground for output short circuit protection. The voltage on NRCS/SCP pin is allowed to recharge up to 1.3 V for short circuit protection after startup. During this start-up period, the voltage on NRCS/SCP is the positive input of the error amplifier in the driving circuit.

SCP

The SCP sense function starts to monitor the output voltage of the LDO once the EN input active high. After the startup, The voltage on NRCS/SCP pin is allowed to recharge up to 1.3 V for short circuit protection. If the LDO is under the output short circuit condition, which output is lower than $0.35 \times V_O$, The external NRCS/SCP capacitor will be recharged up to 1.3 V to activate the SCP by an internal 20 μ A constant current source. During this recharge period, if the output short circuit condition is maintained until the voltage on NRCS/SCP reach 1.3 V, the output will be turned of with latch mode.

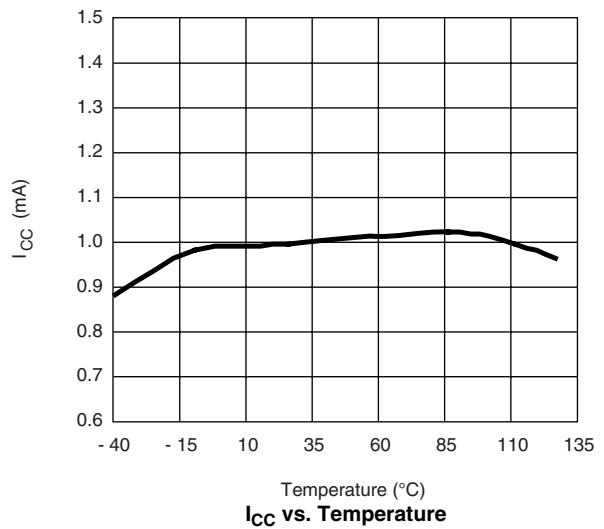
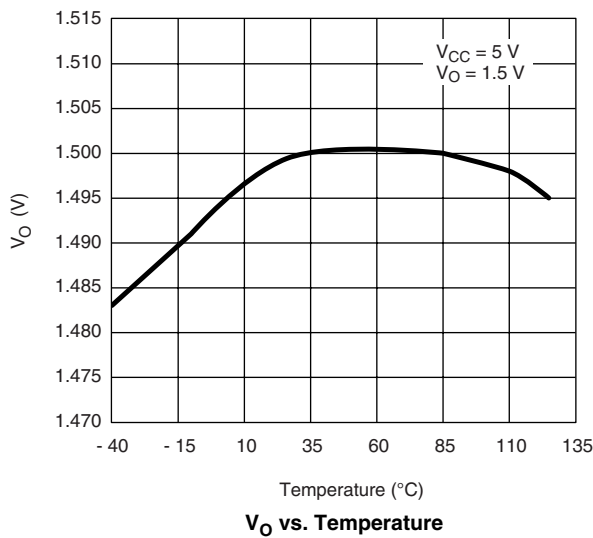
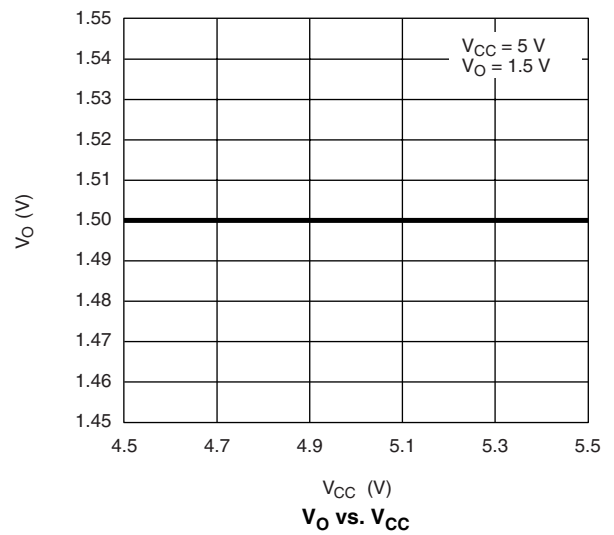
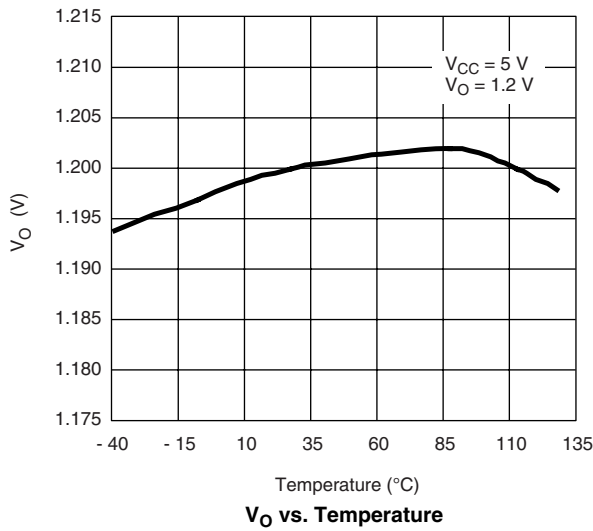
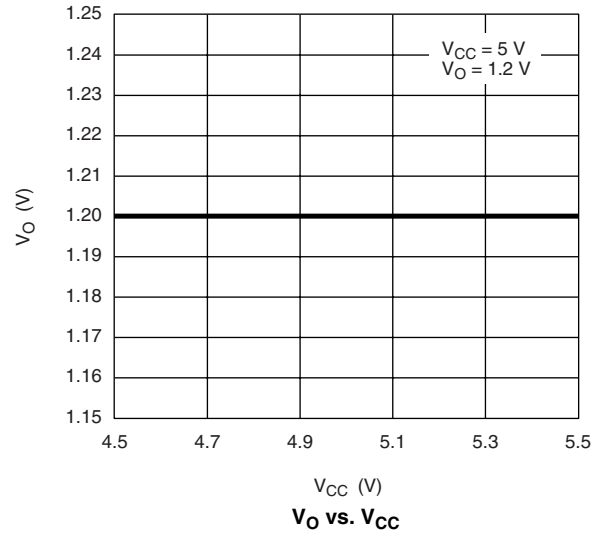
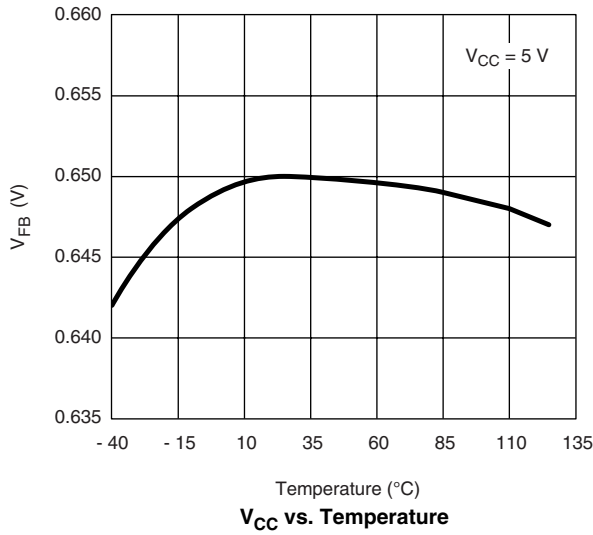
Error Amplifier

The error amplifier is a conventional operation Transconductance amplifier (OTA). This OTA has two positive inputs and one negative input. The negative input as a feedback signal to sense the voltage of LDO output. The LDO output feedback voltage on the negative input of OTA will follow the NRCS/SCP voltage during the start up period. Once the NRCS/SCP voltage exceed the reference voltage (0.65 V) on another positive input of OTA, the feedback voltage on the negative input of the OTA will follow 0.65 V reference voltage to regulate the output voltage of LDO.

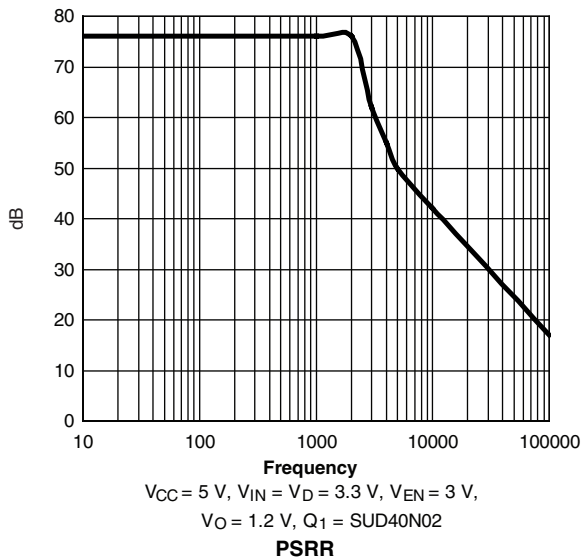
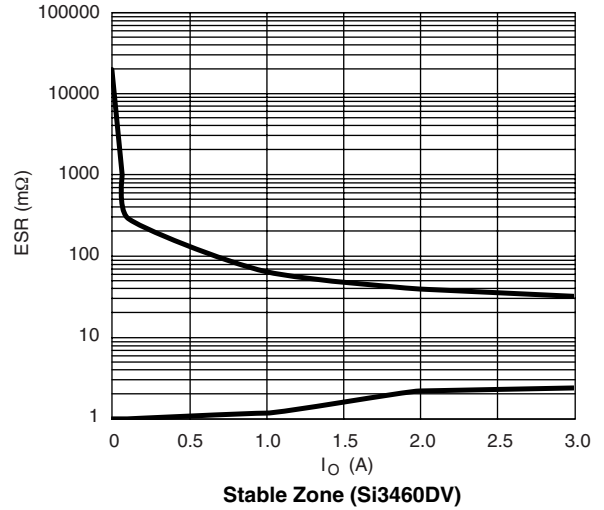
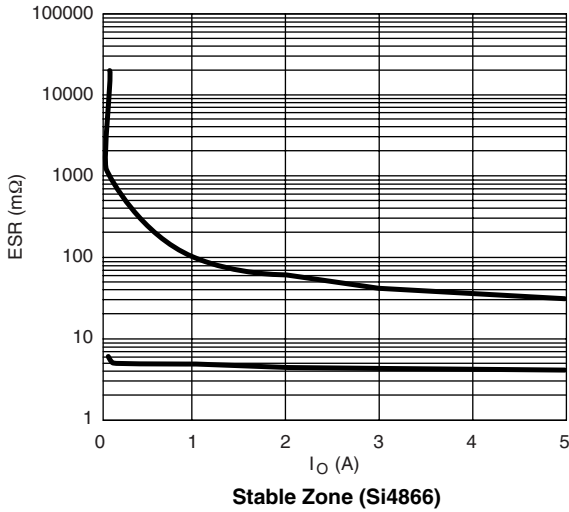
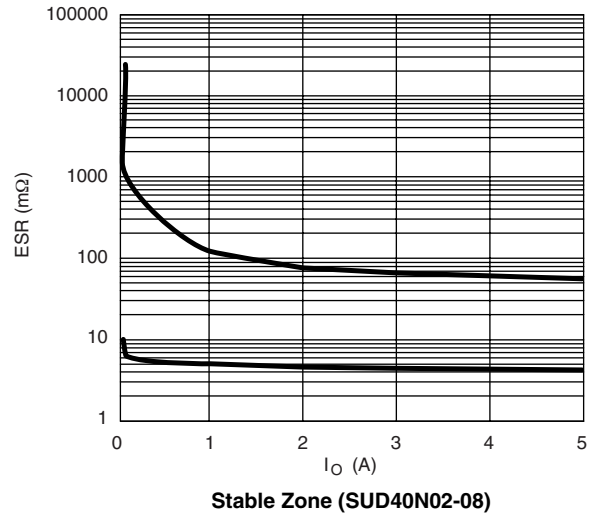
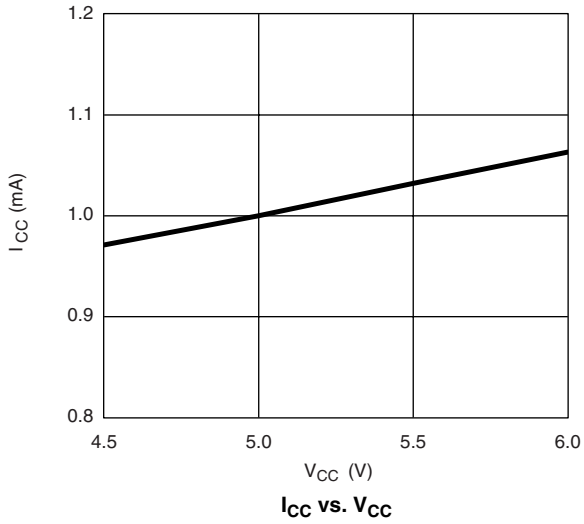
Power Reset

The output short circuit and input power failure will make SiP21301 go into latch shutdown mode. Toggling the EN from its high condition to a low condition, and then back to a high condition can reset an output short circuit latch and input power failure condition.

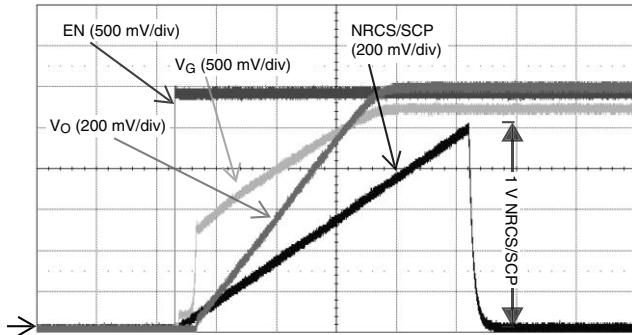
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

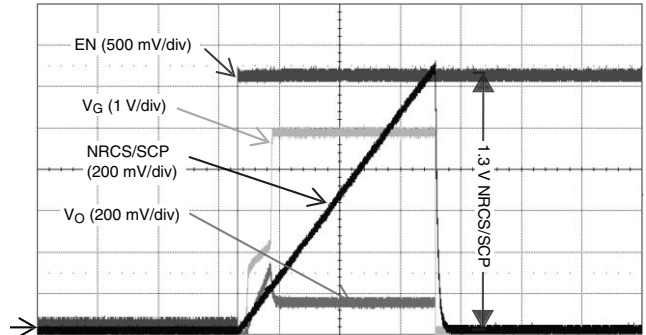


TYPICAL WAVEFORMS



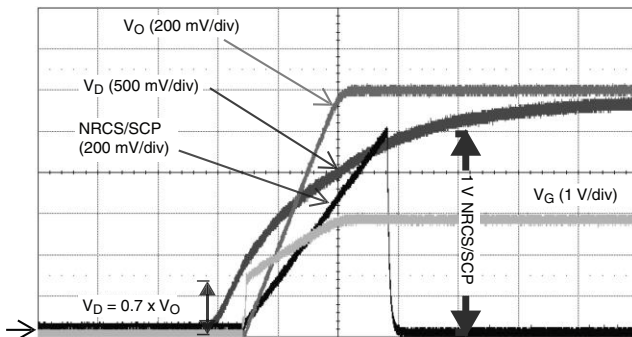
1 ms/div

$V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
EN Pin ENABLE Soft Start-Up



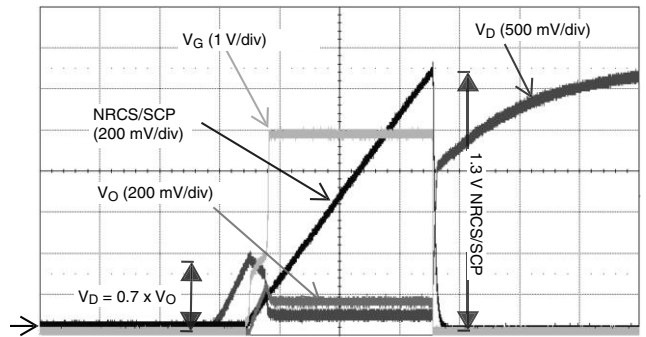
2 ms/div

$V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
EN Pin ENABLE Start-Up with Output Short



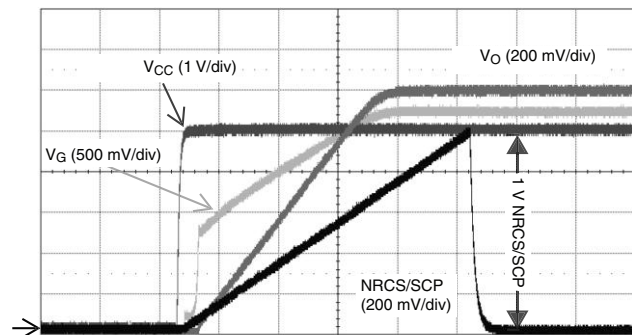
2 ms/div

$V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
Power-In Soft Start-Up



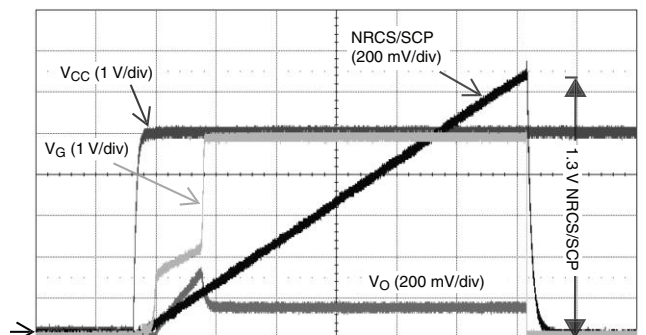
2 ms/div

$V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
Power-In Soft Start-Up with Output Short



1 ms/div

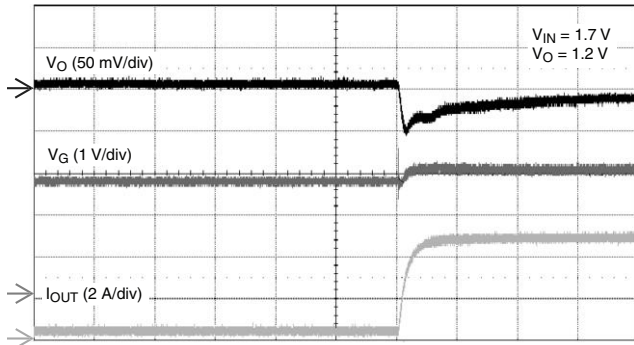
$V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
VCC Power-In Soft Start-Up



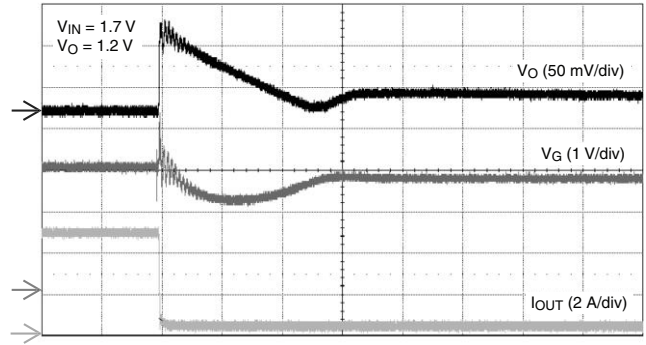
1 ms/div

$V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
VCC Power-In Soft Start-Up with Output Short

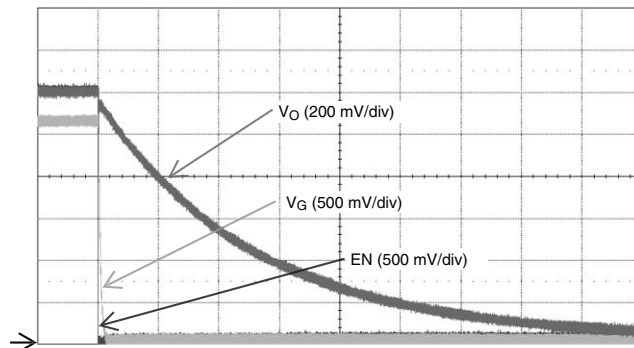
TYPICAL WAVEFORMS



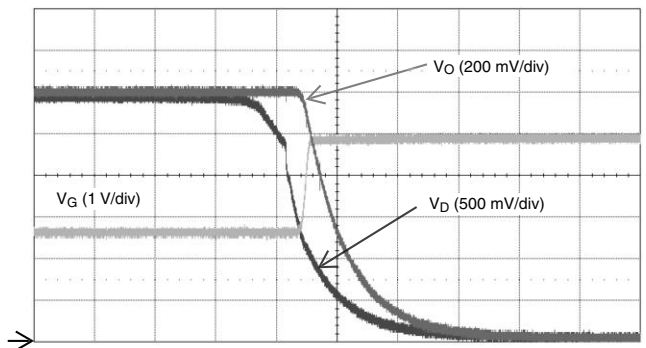
50 μ s/div
 $V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 1.7\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
Rising Edge of Transient Response



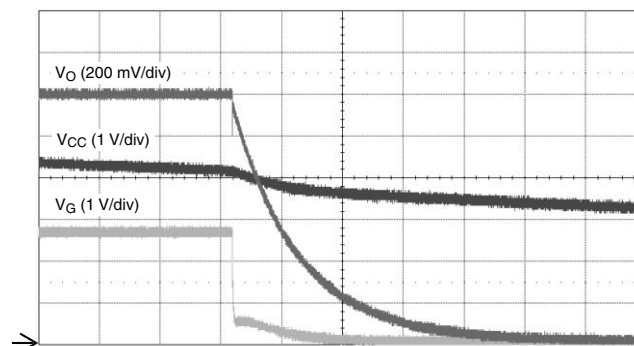
20 μ s/div
 $V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 1.7\text{ V}$, $V_{EN} = 3\text{ V}$,
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Falling Edge of Transient Response



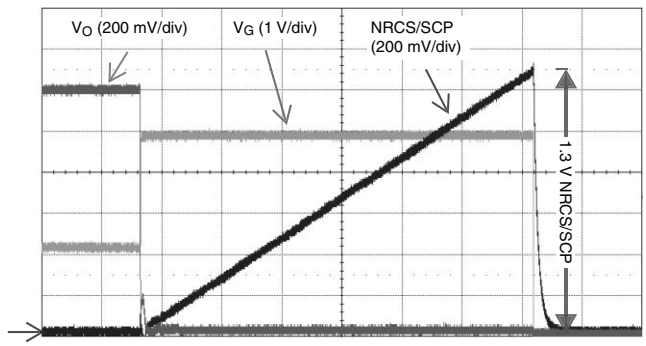
20 μ s/div
 $V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
EN Active Low Power Down



200 μ s/div
 $V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
Input Power Fail



50 μ s/div
 $V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
V_{CC} Power Fail



1 ms/div
 $V_{CC} = 5\text{ V}$, $V_{IN} = V_D = 3.3\text{ V}$, $V_{EN} = 3\text{ V}$,
 $V_O = 1.2\text{ V}$, $I_O = 5\text{ A}$, Q1 = SUD40N02
Output Short Circuit After Start-Up

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