Addressing the New Challenges of Silicon Test

Joe Sawicki
Vice President and General Manager
Design-to-Silicon Division
Why We’re Here

- Describe new silicon test challenges facing the industry
- Explain how Mentor is investing to meet these new challenges
- Share our vision of the Tessent™ platform—Mentor’s comprehensive test and yield analysis solution
- Announce the new Tessent YieldInsight™ product—a unique and innovative approach for improving silicon yield and quality
Agenda

- Critical IC test challenges facing the industry
- Mentor’s silicon test strategy
  - Investing in test technology
  - How Mentor innovation reduces the cost of test
  - New solution initiatives
    - An integrated test platform for SoCs
    - Silicon bring-up and yield analysis solutions
- New product introduction: Tessent YieldInsight
  - Yield analysis challenges
  - Diagnosis-driven yield analysis
  - Statistical analysis with Tessent YieldInsight
  - YieldInsight case study—finding the cause of systematic yield loss
  - The Tessent™ product line
Test Cost Driver
Exploding Test Data Volume

Volume of Test Data and Test Time (relative)

- stuck-at
- at-speed
- other

New tests added to detect new defects at advanced nodes
At-speed test added due to increased timing and SI sensitivity
Traditional tests growing due to increasing gate count

More test patterns → higher test costs → higher production costs
Need for Compression Continues to Grow

Test Data Volume Compression Requirements

Source: ITRS 2007, Test and Test Equipment
Test Cost and TTM Drivers

Test Complexity is Overwhelming

How do you manage all the IP, tools, interfaces and interactions?

Test Challenges
Yield Issues in Nanometer Technologies

Random

Parametric

Systematic

Test Challenges
Evolution of Yield Loss Contributors

Source: Conquering Process Variability (ISSM 2006), A. Strojwas, PDF Solutions, Inc.
Analog/Mixed Signal Test

- Adhoc manual and custom techniques dominate
- Mixed-signal portion of test time increasing at faster rates than digital
System-in-Package (SiP) & 3D Integration

- Limited test access
- Complex through-silicon via structures
- New defect types
- Off-chip memory

Requires...
- Low pin count test methods and standard interfaces
- Via continuity and delay testing
- New fault models
- Off-chip memory BIST

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Mentor Investing in Silicon Test

May 2008

Mentor Graphics Announces Partnership with NXP Semiconductors for Design-for-Test Tools and Technology

WILSONVILLE, Ore., May 6, 2008 – Mentor Graphics Corporation (Nasdaq: MENT) today announced a partnership with NXP Semiconductors in which Mentor’s Design-for-Test (DFT) products will be used by NXP Semiconductors to further improve the quality and time-to-market of NXP’s solutions. The agreement provides NXP with Mentor’s market- and technology-leading DFT solutions, including the TestKompress® compressed pattern generation and the YieldAssist™ failure diagnosis tools. It also provides interim support for NXP’s test tools.

As part of the overall deal…

- Mentor took over the NXP Hamburg DFT development team
- Mentor acquires access to Philips/NXP developed DFT technology

August 2009

Mentor Graphics Acquires LogicVision; Unites BIST, ATPG and Test Pattern Compression Technologies

WILSONVILLE, Ore. and SAN JOSE, Calif., August 18, 2009 – Mentor Graphics Corporation (NASDAQ: MENT) and LogicVision, Inc. (NASDAQ: LGVN) today announced that LogicVision stockholders have voted to approve, and the parties have closed, the previously-announced merger. Former LogicVision stockholders will receive 0.2068 share of Mentor Graphics common stock in exchange for each share of LogicVision common stock.
LogicVision Acquisition
Combining and Building on #1 Market Positions

Figure R-14: ATPG Market Share 2007

- SynTest Technologies: 2%
- Credence Systems: 2%
- Synopsys: 16%
- Cadence Design Systems: 22%
- Mentor Graphics: 58%

(Source: Gary Smith EDA, September 2008)

Figure R-18: BIST Market Share 2007

- SynTest Technologies: 4%
- Genesys Testware: 9%
- Credence Systems: 12%
- Mentor Graphics: 23%
- LogicVision: 52%

(Source: Gary Smith EDA, September 2008)

Overall DFT Market

- Synopsys: 16%
- Mentor + LV: 53%
- Cadence: 8%
- Other: 23%
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Industry Leading ATPG and Compression for High Quality Test

100X compression of test data volume and time
Automatic Test Equipment
Capital Cost per IC Unit (Learning Curve)

Note: ATE Capital Cost Using 3-year straight-line depreciation, Adjusted for Inflation
Source: SIA, VLSI Research, Federal Reserve
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Combining Best-in-Class Point Tools for a Comprehensive Test Solution

ATPG  Layout-Aware Diagnosis
Yield Analysis  Embedded Compression

Logic BIST  Memory BIST
Mixed-Signal BIST  Interactive Debug

Tessent™
Comprehensive Silicon Test Solutions
Mentor’s Silicon Test Solution
Taking a Holistic View of the Design and Process

Tessent

Interactive Test Debug
Layout-Aware Diagnosis
Diagnosis-Driven Yield Analysis

Initiatives
Integrated SoC Test Flow
Single Flow for BIST and/or ATPG & Compression

- RTL checking of DFT rules
- One step DFT IP generation and insertion at core or chip level
- Automatic generation of manufacturing test patterns
- Complete verification at both core and chip
Memory/Logic Built-in Self-Test Products

Tessent MemoryBIST

- Fully embedded solutions with access through standard TAP or CPU interface
- Support for automated eFuse-based repair of embedded memory
- Complete RTL-based IP generation and insertion and verification flow
- Post manufacturing test update

Tessent LogicBIST
Mixed-Signal/High-Speed IO Test Products

- Faster test times and lower test cost
- Accurate picosecond measurements of all critical characteristics
- Complete RTL-based IP generation and insertion and verification flow

Tessent PLLTest

Tessent SerdesTest

Silicon Learning Products

**Tessent SiliconInsight**
- Accelerate silicon validation and test debug
- Interactive bench top or ATE environment

**Tessent Diagnosis**
- Effectively classify and localize silicon defects
- Enables diagnosis-driven yield analysis

**Tessent YieldInsight**
- Reduce cycle time to root cause
- Improve success rate of failure analysis
- Prioritize yield enhancement efforts
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Yield Analysis Challenges

- Identify/isolate observable yield loss
  - Accelerate yield ramp
  - Accelerate excursion resolution
- Identify hidden yield limiters
  - Increase mature yield
  - Increase product quality
Diagnosis-Driven Yield Analysis

Tessent Diagnosis
- Detailed analysis of each failing die
- High resolution/accuracy
- Additional fault isolation tools for FA

Tessent YieldInsight
- Statistical analysis of diagnosis data
- Indicate presence of systematic defects
- Visualization and drill-down capability
Tessent Diagnosis

Layout-Aware Failure Diagnosis

- **Bridging Defects**
  - > 85% reduction in possible suspects

- **Open Defects**
  - > 70% of net segments eliminated as suspects
**Layout-Aware Diagnosis Silicon Example**

**Logical Diagnosis**
- Suspect type: OPEN or DOM BRIDGE
- Possible Bridges: 99
- Possible Open Segments: 14
- Suspect area: 1,192μm²

**Layout-Aware Diagnosis**
- Suspect types: 1 (OPEN)
- Possible Bridges: 0
- Possible Open Segments: 1
- Suspect area: 130μm²
Layout-Aware Diagnosis Silicon Example

Logical Diagnosis

■ Suspect type: OPEN or DOM BRIDGE
■ Possible Bridges: 99
■ Possible Open Segments: 14
■ Suspect area: 1,192μm^2

FA result
M3 open on net n10909 (990.82, 205.235)

Layout-Aware Diagnosis

■ Suspect types: 1 (OPEN)
■ Possible Bridges: 0
■ Possible Open Segments: 1
■ Suspect area: 130μm^2
Introducing Tessent YieldInsight

Diagnosis-Driven Yield Analysis

- Statistical analysis of yield loss
- Automated identification of systematic issues
- Filtering, visualization and drill-down capabilities
Tessent YieldInsight Case Study

Finding Hidden Systematic Yield Loss

- 95 lots
- Layout-aware diagnosis results from ~1400 failing die
- Typical yield analysis does not show significant signature
Via Macro Pareto

Number of failing die where defect segment includes specific via macros

Example of zonal analysis
Via Macro Pareto

Number of failing die where
defect segment includes
specific via macros
### Die / Lot Diagnosed to Contain Single Via5

Number of failing die where defect includes single Via5.
# Die / Lot Diagnosed to Contain Single Via5

The lots with the most occurrences of identified systematic issue are not the lots with the most failing die.
Suspect Net and Defect Bounding Box
**Suspect Net and Defect Bounding Box**

- Suspect OPEN segment
- Only possible single via (M6_M5H)
- Double via
Tessent YieldInsight Case Study

Summary

- Diagnosis-driven yield analysis correctly called out systematic yield limiting issue (*defective via validated by customer*)
- Customer took corrective action with a manufacturing process change to avoid future yield excursions
Uncover Hidden Yield Limiters

Current flow

1. Collect fail data (100-200 failures)
2. Diagnosis on all devices (20-30)
3. Fine phys. loc. (20-30 devices)
4. Construction analysis (20-30)
5. Identify systematic issues

Proposed flow

1. Collect fail data (1,000-2,000)
2. Diagnosis on all devices
3. Zonal analysis
4. Identify devices
5. Identify systematic issues
6. Construction analysis (2-3)
Uncover Hidden Yield Limiters

Current flow

1. Collect fail data (100-200 failures)
2. Diagnosis online (all devices)
3. Physical localization (2000 devices)
4. Construction analysis (20-30 days)
5. Identify systematic issues

Proposed flow

1. Collect fail data (1000-2000 failures)
2. Diagnosis on all devices
3. Zonal analysis
4. Identify devices and systematic issues
5. Construction analysis (2-3 days)

- Reduce time to root cause from weeks to days
- Eliminate costly physical localization
- Identify yield limiters that may otherwise have gone unnoticed
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The Tessent Product Line

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A comprehensive solution to address the new challenges of silicon test and yield analysis
Summary

- Mentor is investing to meet the new challenges of silicon testing
- Tessent provides the industry’s most advanced and comprehensive test solution
- New Tessent YieldInsight product offers a unique and innovative approach for improving silicon yield and quality